What is claimed is:

1. A fault tolerant computer comprising:

a plurality of CPU (Central Processing Unit) modules processing the same instruction string while maintaining clock synchronization;

a plurality of I/O modules each having a plurality of device controllers each executing input/output control processing for a device; and

a transaction synchronization controller, provided in each of said device controllers, that checks if sequences of I/O transactions issued from said plurality of CPU modules match and, if the sequences match, judges that an out-of-synchronization condition is not caused.

2. The fault tolerant computer according to claim 1 wherein said transaction synchronization controller comprises:

timer means for measuring a predetermined time; and

comparison means for checking if the sequences of I/O transactions, issued from the plurality of CPU modules, match on a device controller basis while waiting for the predetermined time.

3. The fault tolerant computer according to claim 2 wherein said transaction synchronization controller further comprises an output controller that outputs said I/O transactions to said device controller when said sequences match.

4. The fault tolerant computer according to claim 3 wherein,

when the I/O transactions from the CPU modules match, said output controller outputs the matching I/O transactions to said device controller, one at a time.

5. The fault tolerant computer according to claim 2 wherein, when the sequences do not match within the predetermined time or when the sequences of I/O transactions differ, said output controller outputs a failure notification.

6. The fault tolerant computer according to claim 2, further comprising a plurality of storage means in which the I/O transactions issued from said plurality of CPU modules are stored.

7. The fault tolerant computer according to claim 2 wherein said transaction synchronization controller further comprises selection circuits that select between said plurality of storage means and said CPU modules as a source from which I/O transactions to be sent to said comparison means are received.

8. A transaction synchronization control method for use in a fault tolerant computer, said method comprising:

a first step of sending a plurality of, and the same, I/O transactions from a plurality of CPU modules, which process the same instruction string while maintaining clock synchronization, to an I/O module; and

a second step of checking if sequences of the received I/O transactions match in each of a plurality of device

controllers provided in said I/O module and, if the sequences match, judging that an out-of-synchronization condition is not caused.

9. The transaction synchronization control method according to claim 8 wherein said second step checks if the sequences of I/O transactions match while waiting for a predetermined time.

10. The transaction synchronization control method according to claim 9, further comprising a third step of outputting the I/O transactions to said device controller when the sequences match.

11. The transaction synchronization control method according to claim 9 wherein, for each device controller, said first step stores the I/O transactions issued from said plurality of CPU modules into a plurality of storage means and

wherein said second step sends the I/O transactions, received from the CPU modules, to comparison means for use in comparing the I/O transactions, checks if the predetermined time has elapsed if the I/O transactions do not match, and judges that an out-of-synchronization condition is not caused if the predetermined time has not yet elapsed.

12. The transaction synchronization control method according to claim 11 wherein, when the received I/O transactions match, the matching I/O transactions are output to said device controller, one at a time.

13. The transaction synchronization control method according to claim 9, further comprising the step of outputting a failure notification when the sequences do not match within the predetermined time.

14. The transaction synchronization control method according to claim 11, further comprising the step of selecting between said plurality of storage means and said CPU modules as a source when a new I/O transaction is sent to said comparison means.

15. The transaction synchronization control method according to claim 14 wherein, when the storage means do not contain effective data, said step of selecting between said plurality of storage means and said CPU modules switches the source to the CPU modules.

16. A transaction synchronization control program product for use in a fault tolerant computer in which the same instruction string is processed by a plurality of CPU modules while maintaining clock synchronization, said program product comprising:

a first step of sending a plurality of, and the same, I/O transactions from the plurality of CPU modules to an I/O module; and

a second step of checking if sequences of the received I/O transactions match in each of a plurality of device controllers provided in said I/O module and, if the sequences

match, judging that an out-of-synchronization condition is not caused.

17. The transaction synchronization control program product according to claim 16 wherein said second step checks if the sequences of I/O transactions match while waiting for a predetermined time.

18. The transaction synchronization control program product according to claim 17, further comprising a third step of outputting the I/O transactions to said device controller when the sequences match.

19. The transaction synchronization control program product according to claim 16, further comprising the step of outputting a failure notification when the sequences do not match within the predetermined time or when the sequences of I/O transactions differ.

20. The transaction synchronization control program product according to claim 17

wherein, for each device controller, said first step comprises the step of storing the I/O transactions, issued from said plurality of CPU modules, into a plurality of storage means and

wherein said second step comprises the steps of sending the I/O transactions received from the CPU modules to comparison means and comparing the I/O transactions; checking if the

predetermined time has elapsed if the I/O transactions do not match; and judging that an out-of-synchronization condition is not caused when the predetermined time has not yet elapsed.